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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,417	10/20/2003	Warren M. Farnworth	2269-5947US (03-0316.00/U	3773

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,417	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *40-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19-37 and 39* is/are rejected.

7)☒ Claim(s) *18 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/03, 12/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 20 October 2005. Claims 1-45 are pending.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-39, drawn to a method of making a semiconductor device, classified in class 438, subclass 106.

II. Claims 40-45, drawn to a semiconductor device, classified in class 257, subclass 678.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process, such as by separating a semiconductor wafer into a plurality of semiconductor die and then providing each die with protective coatings.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Joseph Walkowski (Reg. No. 28,765) on 7 January 2005 a provisional election was made without traverse to prosecute the invention of group I, claims 1-39. Affirmation of this election must be made by applicant in replying to this Office action. Claims 40-45 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 8, 19-22, 28 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (5,977,641) in view of Shelton et al. (6,849,524).

Takahashi et al. disclose a method of forming chip-scale packages including providing a semiconductor wafer (1) having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material (Fig. 3A); cutting at least one channel (16) in the active surface of the semiconductor

wafer (1) along the at least one street of semiconductor material to expose a plurality of semiconductor die surfaces (Fig. 3C); forming a protective coating (12) on the semiconductor wafer (1) to cover the active surface and fill the at least one channel (16) (Fig. 4A); and separating the semiconductor wafer (1) along the at least one channel (16) to form a plurality of individual chip-scale packages (Fig. 4C). Takahashi et al. do not disclose forming a first protective coating on the semiconductor wafer; and etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects.

Shelton et al. disclose a method of forming chip-scale packages including providing a semiconductor wafer having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material; forming a protective coating on the semiconductor to cover the active surface (step 410); cutting at least one channel in the active surface of the semiconductor wafer along the at least one street of semiconductor material to expose a plurality of semiconductor die surfaces (Step 440); etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects (Step 550); and separating the semiconductor wafer along the at least one channel to form a plurality of individual chip-scale packages (Step 560).

Since Takahashi et al. and Shelton et al. are both from the same field of endeavor, a method of forming chip-scale packages, the purpose disclosed by Shelton et al. would have been recognized in the pertinent art of Takahashi et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to modify Shelton et al. by forming a protective coating on the semiconductor to cover the active surface and etching the plurality of semiconductor die side surfaces to remove a layer of semiconductor material containing cutting-induced defects as taught by Shelton et al. to increase yields (col. 1,lines 48-60).

Referring to claims 2 and 22, Shelton et al. disclose cutting at least one channel in the active surface of the semiconductor wafer comprises cutting the at least one channel with one of a dicing saw and a laser beam (col. 4, lines 22-26).

Referring to claims 8 and 28, Takahashi et al. disclose each semiconductor die location of the plurality includes at least one bond pad (13) and forming a conductive bump (14) on the at least one bond pad (13) of each semiconductor die location (col. 7, lines 33-50).

Referring to claim 19, Takahashi et al. disclose each semiconductor die location of the plurality of semiconductor die locations comprises a plurality of circuit layers extending a depth into the semiconductor wafer from the active surface of the semiconductor wafer, and wherein cutting at least one channel in the active surface of the semiconductor wafer comprises cutting the at least one channel to a depth that is greater than the depth of the circuit layers within the semiconductor wafer (col. 7, lines 5-8).

Referring to claims 20 and 39, Shelton et al. disclose etching the plurality of semiconductor die side surfaces comprises etching the plurality of semiconductor die side surfaces with KOH, an anisotropic etching agent.

Claims 3-5, 9-11, 23-25 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. in view of Shelton et al. as applied to claims 1 above, and further in view of Chung (6,399,178).

Takahashi et al. in view of Shelton et al. disclose the subject matter claimed above except forming the protective coating on the semiconductor wafer by applying a liquid polymer material over the active surface of the semiconductor wafer; at least partially curing the liquid polymer material; applying the liquid polymer material by spraying or spin coating; forming the conductive bump prior to forming the first protective coating on the semiconductor wafer.

Referring to claims 9 and 29, Chung discloses a method of forming chip-scale packages including providing a semiconductor wafer (30) having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material; each semiconductor die including at least one bond pad (32); forming a conductive bump (34) on the at least one bond pad (32); and forming a protective layer (12) on the semiconductor wafer to cover the active surface.

Referring to claims 3, 10, 23 and 30, Chung discloses forming the protective coating (12) on the semiconductor wafer by applying a liquid polymer material over the active surface of the semiconductor wafer; and at least partially curing the liquid polymer material (col. 22, lines 44-59).

Referring to claims 4 and 24, Chung discloses applying the liquid polymer material by spraying or spin coating (col. 22, lines 44-59).

Since Takahashi et al. and Chung are both from the same field of endeavor, a method of forming chip-scale packages, the purpose disclosed by Chung would have been recognized in the pertinent art of Takahashi et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takahashi et al. by forming the protective coating on the semiconductor wafer by applying a liquid polymer material over the active surface of the semiconductor wafer; at least partially curing the liquid polymer material; applying the liquid polymer material by spraying or spin coating; forming the conductive bump prior to forming the first protective coating on the semiconductor wafer as taught by Chung to obtain good thermal conductivity (col. 6,lines 5-27).

Referring to claims 5, 11, 25 and 31, Takahashi et al. disclose etching a portion of the protective coating (32) to expose the at least one bond pad (31) of the semiconductor die (Fig. 6D; col. 8, lines 51-59).

Claims 6, 7, 12, 13, 26, 27, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. in view of Shelton et al. in further view of Chung as applied to claims 1, 3, 9, 21, 23 and 29 above, and further in view of Luo et al. (6,885,108).

Takahashi et al. in view of Shelton et al. in further view of Chung disclose the subject matter claimed above except the liquid polymer material comprises a photocurable liquid polymer material and exposing the photocurable liquid polymer

material to a source of electromagnetic radiation to at least partially cure a portion of the photocurable liquid polymer material.

Luo et al. disclose a method of forming chip-scale packages including providing a semiconductor wafer (12) having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material; each semiconductor die including at least one bond pad (16); forming a conductive bump (18) on the at least one bond pad (16); and forming a protective layer (20) on the semiconductor wafer to cover the active surface.

Referring to claims 6, 12, 26 and 32, Luo et al. disclose the liquid polymer material comprises a photocurable liquid polymer material and exposing the photocurable liquid polymer material to a source of electromagnetic radiation to at least partially cure a portion of the photocurable liquid polymer material (col. 5, lines 49-55).

Since Takahashi et al. and Luo et al. are both from the same field of endeavor, a method of forming chip-scale packages, the purpose disclosed by Luo et al. would have been recognized in the pertinent art of Takahashi et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takahashi et al. by the liquid polymer material comprises a photocurable liquid polymer material and exposing the photocurable liquid polymer material to a source of electromagnetic radiation to at least partially cure a portion of the photocurable liquid polymer material as taught by Luo et al. so the polymer will facilitate cutting but also allow flow (col. 5, lines 55-63).

Referring to claims 7, 13, 27 and 33, Takahashi et al. disclose selectively curing the photocurable liquid polymer material to leave the at least one bond pad of each semiconductor die location exposed through the first protective coating (col. 8, lines 8-17).

Claims 14-16 and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. in view of Shelton et al. as applied to claim 1 above, and further in view of Ohuchi et al. (6,353,267).

Takahashi et al. in view of Shelton disclose the subject matter claimed above except the semiconductor wafer has a passive surface opposite the active surface, removing a layer of semiconductor material from the passive surface of the semiconductor wafer to a depth sufficient to expose the first protective coating within the at least one channel; and forming a second protective coating on the semiconductor wafer to cover the passive surface, wherein removing the layer of semiconductor material comprises planarizing the passive surface of the semiconductor wafer with at least one of a mechanical process and a chemical process, wherein removing the layer of semiconductor material comprises back grinding the passive surface of the semiconductor wafer.

Ohuchi et al. disclose a method of forming chip-scale packages including providing a semiconductor wafer (30) having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material; each semiconductor die including at least one bond pad (31); forming a protective layer

(32) on the semiconductor wafer to cover the active surface; and cutting at least one channel (35) in the active surface of the semiconductor wafer to expose a plurality of semiconductor die surfaces.

Referring to claim 14, Ohuchi et al. disclose wherein the semiconductor wafer (30) has a passive surface opposite the active surface, removing a layer of semiconductor material from the passive surface of the semiconductor wafer (30) to a depth sufficient to expose the first protective coating (32) (Fig. 4-B); and forming a second protective coating (38) on the semiconductor wafer (30) to cover the passive surface (FIG. 4-C).

Referring to claims 15 and 35, Ohuchi et al. disclose removing the layer of semiconductor material comprising planarizing the passive surface of the semiconductor wafer with at least one of a mechanical process and a chemical process.

Referring to claims 16 and 36, Ohuchi et al disclose removing the layer of semiconductor material comprising back grinding the passive surface of the semiconductor wafer (30).

Referring to claim 34, Ohuchi et al. disclose removing a layer of semiconductor material from the passive surface of the semiconductor wafer prior to forming a second protective coating on the semiconductor wafer (30).

Since Takahashi et al. and Ohuchi et al. are both from the same field of endeavor, a method of forming chip-scale packages, the purpose disclosed by Ohuchi et al. would have been recognized in the pertinent art of Takahashi et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was

made to modify Takahashi et al. by [how modified] as taught by Ohuchi et al. to form individual devices (col. 4, lines 45-49).

Claims 17 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. in view of Shelton et al. further in view of Ohuchi et al. as applied to claims 1 and 14 above, and further in view of Farnworth et al. (6,620,731).

Takahashi et al. in view of Shelton et al. further in view of Ohuchi et al. disclose the subject matter claimed above except removing the layer of semiconductor material using CMP process.

Farnworth et al. disclose a method of forming chip-scale packages including providing a semiconductor wafer (10A) having an active surface with a plurality of semiconductor die locations separated by at least one street of semiconductor material; each semiconductor die including at least one bond pad (18A); forming a protective layer (20A) on the semiconductor wafer to cover the active surface; and cutting at least one channel (30A) in the active surface of the semiconductor wafer (10A) to expose a plurality of semiconductor die surfaces, wherein the semiconductor wafer (10A) has a passive surface opposite the active surface, removing a layer of semiconductor material from the passive surface of the semiconductor wafer (10A) to a depth sufficient to expose a protective coating (34A); and forming a second protective coating (42A) on the semiconductor wafer (10A) to cover the passive surface (FIG. 4-C).

Referring to claims 17 and 37, Farnworth et al. disclose removing the layer of semiconductor material using a CMP process.

Since Takahashi et al. and Farnworth et al. are both from the same field of endeavor, a method of forming chip-scale packages, the purpose disclosed by Farnworth et al. would have been recognized in the pertinent art of Takahashi et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Takahashi et al. by removing the layer of semiconductor material using a CMP process as taught by Farnworth et al. to control the thinning process (col. 8, lines 61-67).

Allowable Subject Matter

Claims 18 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: referring to claim 18, prior art does not disclose teach or suggest etching the passive surface of the semiconductor wafer such that the first protective coating exposed within the at least one channel forms at least one frame element protruding from the passive surface of the semiconductor wafer; and anchoring the second protective coating to the passive surface of the semiconductor wafer with the at least one frame element.

Referring to claim 38, prior art does not disclose teach or suggest etching the passive surface of the semiconductor wafer concurrently with etching the plurality of semiconductor die side surfaces.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Murphy (3,978,578) and Zandman et al. (6,562,647) both disclose forming a channel in a semiconductor wafer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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